REMARKS

This amendment is a full and timely response to the Final Office Action dated September 15, 2010. Claims 1-6 are pending, with claims 1, 3, and 5 being independent. In this amendment, claims 1-6 have been amended. Support for these amendments is variously found in the Applicant's specification as filed, including but not necessarily limited to the paragraphs (¶¶) of the specification cited below, as represented in U.S. Pub. No. 2006/0152461 A1. Reconsideration and allowance is requested in view of the following remarks. *No new matter has been added by these amendments.*

Claims 1-2 and 5-6 have been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by *Edwards*, U.S. Patent Number 6,498,438 (*Edwards*). This rejection is respectfully traversed.

Independent claim 1, as amended, recites "[*a*] *method for operating a constant current circuit, comprising: after connecting a sampling capacitor connected between a gate and a source of a first transistor and a drain of the first transistor to a reference current source and setting a voltage across the sampling capacitor to a voltage between the gate and the source produced while the first transistor is driven by a reference current of the reference current source, cutting off the connection among the sampling capacitor, the first transistor and the reference current source, as well as connecting the drain of the first transistor to a buffer circuit, and driving the buffer circuit by a current of the first transistor due to the voltage between the gate and the source that is set in the sampling capacitor, wherein said cutting off the connection comprises applying a first signal to a gate of a second transistor connected between the drain of the first transistor and the reference current source, a second signal that is a logical inverse of said first signal to a gate of a third transistor connected between the gate and drain of the first transistor, and a third signal to a gate of a fourth transistor connected between the drain of the first transistor and the buffer circuit, wherein said setting the voltage across the sampling capacitor and said cutting off the connection occur within a precharge period to cause the constant current circuit to be temporarily connected to a source of a buffer circuit transistor of the buffer circuit during the precharge period.*"

Edwards fails to disclose or suggest these claimed features. *Edwards* discloses a circuit 40 for producing an output current (at output 50) from an input word using switching transistors, and

managing this output current via a transistor 70 in FIG. 6 (or T1 in FIG. 8) for resetting the voltage and a four transistor arrangement (T2 – T5) for avoiding a large voltage ramp at output 50. (*Edwards*, FIGs. 4-5c and 7d-8).

Edwards, in its four transistor arrangement, specifically uses a single sample line to turn transistors T2 and T3 on and off thereby forcing both transistors T2 and T3 to be in the same logic state as dictated by the sample line. (*Edwards*, col. 9 line 2). Furthermore, this four transistor arrangement outputs directly to the column such that the current drive output does not have a large voltage ramp. (*Edwards*, col. 9 lines 10-11).

In contrast to *Edwards*, Applicant's "*constant current circuit is . . . connected to a source of a buffer circuit transistor of the buffer circuit.*" Further, Applicant's timing signals (which as described below are clearly distinct from the timing signals in *Edwards*) control the current paths during a period for "*setting the voltage across the sampling capacitor and ... cutting off the connection occur within a precharge period to cause the constant current circuit to be temporarily connected to a source of a buffer circuit transistor of the buffer circuit during the precharge period.*" Accordingly, the constant current circuit is held in the state of inhibiting the buffer transistor from discharging any current. (U.S. Publication 2006/0152461 A1, Specification ¶ [0050]).

More clearly, Applicant's constant current circuit is connected with the source of the buffer circuit transistor through its fourth transistor such that the fourth transistor permits a current to flow in and out. The sampling capacitor maintains a gate source voltage for a first transistor so the driving current may drive the buffer circuit, i.e. the driving circuit may flow in and out to of the fourth transistor while the current remain constant. **Thus, while *Edwards* prevents voltage ramping, Applicant claims a buffer circuit that can not discharge due to the constant current circuit.**

Consistent with these distinctions, Applicant applies separate first, second, and third signals (*a first signal ..., a second signal ..., and a third signal"*) to connect and cut off the constant current circuit to the reference current and the buffer circuit ("*the constant current circuit* [*is*] ... *temporarily connected to a ... buffer circuit*"). In this regard, each transistor may be triggered in

different stages or at different time intervals, rather than always keeping transistors T2 and T3 in the same logic state as is done in *Edwards*. Thus and by way of example, the timing signal xNcnt1 is held at an L level when the timing signals Ncnt2 is held at an H level; the respective logical values of the timing signals xNcnt1 and Ncnt2 are simultaneously switched; and "the respective timing signals xNcnt1, Nact and Ncnt2 are supplied so that the constant current circuit 26 operates . . . to function as a constant current circuit. (U.S. Publication 2006/0152461 A1, Specification ¶¶ [0050] - [0053]).

Accordingly, *Edwards* fails to yield features of Applicant's claimed invention, a prima facie case of obviousness for independent claim 1 has not been presented. For reasons similar to those provided for claim 1, independent claim 5 is also neither disclosed by *Edwards*. The dependent claims are also distinct for their incorporation of the features respectively recited in the independent claims as well as for their own, separately recited patentably distinct features.

Specifically, regarding claim 2, repeating the period when the voltage between terminals of the capacitor for sampling is set in not disclosed in *Edwards*.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1-2 and 5-6 under 35 U.S.C. § 103(a) as being unpatentable over *Edwards*.

Claims 3 and 4 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over *Edwards* and *Yamazaki*, U.S. Publication No. 2006/0267899 (*Yamazaki*). This rejection is respectfully traversed at least for the following reasons.

Similarly to the discussion above, these claimed features are not disclosed or suggested by *Edwards*.

Edwards does not discloses "*a digital-to-analog conversion circuit for performing digital-to-analog conversion processing of gradation data indicative of gradations of the pixels; and a buffer circuit for driving the signal lines by means of an output signal from the digital-to-analog conversion circuit; the buffer circuit drives the signal lines by a source follower circuit formed by connecting a constant current circuit to a source of a transistor*," which the Office Action admits. (Office Action Page 9).

Thus, *Edwards* does not disclose nor in any way suggest the Applicant's claimed features of independent claim 3. *Yamazaki* does not remedy the deficiencies of *Edwards*.

Yamazaki discloses an LCD display that is said to avoid deterioration of the image due to image persistence. *Yamazaki* is relied upon for purported disclosure of a digital to analog conversion circuit, a buffer circuit, and their related features conceded to be absent from *Edwards*. However, *Yamazaki* offers no disclosure or suggestion of the above-described features that are also absent from *Edwards*. In addition, since *Edwards* does not teach or suggest Applicant's claimed features and since *Yamazaki* offers no disclosure or suggestion regarding Applicant's claimed features, an artisan would not be inclined to combine *Yamazaki* with *Edwards*.

Accordingly, since even a combination of *Edwards* and *Yamazaki* would still fail to yield features of Applicant's claimed invention, a prima facie case of obviousness for independent claim 3 has not been presented.

For reasons similar to those provided for claim 3, dependent claim 4 is also distinct for its incorporation of the features respectively recited in the independent claim 3 as well as for its own, separately recited patentably distinct features.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over *Edwards* and *Yamazaki*.

In view of the above amendment, applicant believes the pending application is in condition for allowance. If any further issues remain, the Examiner is invited to telephone the undersigned to resolve them.

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

This response is believed to be a complete response to the Office Action. However, Applicant reserves the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers. Further, for any instances in which the Examiner took Official Notice in the Office

Action, Applicant expressly does not acquiesce to the taking of Official Notice, and respectfully requests that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-3056 from which the undersigned is authorized to draw.

Dated: December 14, 2010

Respectfully submitted,

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